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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/675,831
Filing Date: September 30, 2003
Appellant(s): DEWITT ET AL.

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Technology Center 2100

Gerald H. Glanzman
Reg. No. 25,035
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 24 October 2006 appealing from the Office action mailed 02 June 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claim Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Heisch (U.S. Patent No. 5,774,724)

Embedded Microprocessor Systems Design: An Introduction Using the Intel 80C188EB

(9) Grounds of Rejection

Maintained rejection from final action

Specification

The amendment filed 1 May 2006 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: Striking the disclosure of transmission-type media on pages 64-65

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 8-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Heisch (U.S. Patent No. 5,774,724).

As per claim 1, Heisch discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction for execution in an instruction cache (Fig. 2 cache 60) in a processor in the data

processing system, determining whether a performance indicator that identifies that execution of the instruction is to be monitored is present (Col. 5 lines 58-65); and forcing an interrupt if the performance indicator is present (Col. 5 line 66 – col. 6 line 6). *The examiner asserts that matching the contents of the IABR register to the executing instruction's address constitutes a "performance indicator". Col. 4 lines 13-16 disclose that upon matching a start address to the IABR, performance monitoring is initiated by means of an exception.*

As per claim 2, Heisch discloses the method of claim 1, wherein the forcing step comprises: sending a signal from an instruction cache to an interrupt unit in the processor; and processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit. (Col. 6 lines 2-6) *The examiner asserts that logic comparing the current instruction's address to the address stored in the IAB register constitutes part of the instruction cache. The logic must inherently generate a signal to alert the interrupt handler to a pending interrupt. If no such signal was generated, the interrupt would go unprocessed.*

As per claim 3, Heisch discloses the method of claim 2, wherein the processing step includes: executing code associated with the interrupt. (Col. 6 line 9-13) *The examiner asserts that when control is transferred to another function, code is executed which is associated with that function.*

As per claim 4, Heisch discloses the method of claim 3, wherein the code records cache misses by a functional unit attempting to access instructions in a cache. (Col. 6 lines 21-25) *The examiner asserts that counting cache misses constitutes recording.*

As per claim 5, Heisch discloses the method of claim 1, wherein the performance indicator is located in a shadow memory. (Col. 5 lines 58-65) *The examiner asserts that the IAB register is not located in main memory, and hence, constitutes shadow memory.*

As per claim 8, Heisch discloses a method in a data processing system for processing data, the method comprising: responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present (Col. 5 lines 58-65); and generating an interrupt if the performance indicator is present. (Col. 5 line 66 – col. 6 line 6) *The examiner asserts that the method described by Heisch anticipates causing an interrupt on a data access (Col. 10 line 13-15). The examiner asserts that matching the contents of the IABR register to the address in question constitutes a "performance indicator". Col. 4 lines 13-16 disclose that upon matching a start address to the IABR, performance monitoring is initiated by means of an exception.*

As per claim 9, Heisch discloses the method of claim 8, wherein the generating step comprises: generating a signal by a data cache in which the data is located; and

receiving the signal generated by the data cache at an interrupt unit, wherein the signal indicates a presence of the interrupt to the interrupt unit. (Col. 6 lines 2-6) *The examiner asserts that logic comparing the current access address to the address stored in the IAB register constitutes part of the data cache. The logic must inherently generate a signal to alert the interrupt handler to a pending interrupt. If no such signal was generated, the interrupt would go unprocessed.*

As per claim 10, Heisch discloses the method of claim 8 further comprising: processing the interrupt in an interrupt unit in response to generation of the interrupt. (Col. 6 line 2-6)

As per claim 11, Heisch discloses the method of claim 10, wherein the processing step comprises: executing a code for handling the interrupt. (Col. 6 line 9-13) *The examiner asserts that when control is transferred to another function, code is executed which is associated with that function.*

As per claim 12, Heisch discloses the method of claim 8, wherein the performance indicator identifies that access of the data is to be monitored through a specific value in a memory location for the data. (Col. 5 lines 58-65) *The examiner asserts that the address of interest loaded into the IAB register is a memory location. Col. 10 line 13-15 dictates that the address can be that of data.*

As per claim 13, Heisch discloses the method of claim 8, wherein the data is located in a memory location. *The examiner asserts that an address inherently points to a location in memory.*

As per claim 14, Heisch has taught a processing system performing the method of claim 1, consequently claim 14 is rejected for the same reasons set forth in the rejection of claim 1 above.

As per claim 15, Heisch has taught a processing system performing the method of claim 2, consequently claim 15 is rejected for the same reasons set forth in the rejection of claim 2 above.

As per claim 16, Heisch has taught a processing system performing the method of claim 3, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 3 above.

As per claim 17, Heisch has taught a processing system performing the method of claim 4, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 4 above.

As per claim 18, Heisch has taught a processing system performing the method of claim 8, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 8 above.

As per claim 19, Heisch has taught a processing system performing the method of claim 9, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 9 above.

As per claim 20, Heisch has taught a processing system performing the method of claim 10, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 10 above.

As per claim 21, Heisch has taught a computer program product performing the method of claim 1, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 1 above.

As per claim 22, Heisch has taught a computer program product performing the method of claim 2, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 2 above.

As per claim 23, Heisch has taught a computer program product performing the method of claim 3, consequently claim 23 is rejected for the same reasons set forth in the rejection of claim 3 above.

As per claim 24, Heisch has taught a computer program product performing the method of claim 8, consequently claim 24 is rejected for the same reasons set forth in the rejection of claim 8 above.

As per claim 25, Heisch has taught a computer program product performing the method of claim 9, consequently claim 25 is rejected for the same reasons set forth in the rejection of claim 9 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Short (Short, K. L. "Embedded Microprocessor Systems Design: An Introduction Using the Intel 80C188EB." Prentice-Hall, Inc: 1998. Page 761.) in view of Heisch.

As per claim 1, Short discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether an indicator is present; and forcing an interrupt if the indicator is present. *The examiner asserts that if the opcode of the instruction (indicator) indicates the Interrupt instruction (Short pg. 761), an interrupt will be forced.*

Short fails to disclose wherein the indicator is a performance indicator that identifies that execution of the instruction is to be monitored.

Heisch discloses using a interrupt routine to monitor performance of an instruction in a microprocessor system. (Col. 4 lines 8-18)

Heisch teaches that using an interrupt (exception) routine to handle performance monitoring gives greater flexibility and more detailed information than existing performance monitor systems. (Col. 1-Col. 4)

It would have been obvious to one of ordinary skill in the art at the time of invention to have included Heisch's performance monitoring interrupt handler in Short's processor for the benefit of a detailed and flexible performance monitoring scheme by means of interrupts.

As per claim 6, Short and Heisch disclose the method of claim 1, wherein the instruction is received in a bundle and wherein the performance indicator comprises at least one bit in a field in the bundle. *The examiner asserts that a bundle may contain*

just one instruction. Further, the opcode (indicator) comprises at least one bit in a field in the instruction, which is in the bundle. (Short pg. 761)

As per claim 7, Short and Heisch disclose the method of claim 1, wherein the performance indicator is located in a field in the instruction. *The examiner asserts that the opcode (indicator) comprises at least one bit in a field in the instruction, as detailed by Short on pg. 761.*

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 21-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Pages 64-65 of the specification define "computer readable media" to include "transmission-type media". Transmission media are not tangible, and hence, non-statutory. *The examiner notes that the amendment to the specification filed 1 May 2006 must be cancelled, as it constitutes new matter. In order to overcome this rejection, the examiner recommends amending claims 19-25 to read "A computer program product in a computer readable recordable-type medium..."*

(10) Response to Argument

Applicant's arguments filed 24 October 2006 have been fully considered but they are not persuasive.

Appellant states:

"Appellants respectfully admit that Heisch does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Heisch does not teach or suggest 'responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies the execution of the instruction is to be monitored is present...Examiner refers to col. 5, lines 58-65 of Heisch...Nowhere in [this] recitation, nor anywhere else in Heisch, is there any disclosure or suggestion of making a determination as to whether a performance indicator that identifies that execution of an instruction is to be monitored is present in response to receiving an instruction for execution in an instruction cache in a processor."

Appellant further states:

"[col. 8, lines 16-24 of Heisch] states that cache misses may be counted by the performance monitor 'if it is desired to count cache misses'. This statement suggests that Heisch does not determine whether a performance indicator that identifies the execution of an instruction is to be monitored is present before forcing an interrupt and supports Appellants' assertion that Heisch does not disclose or suggest 'responsive to receiving an instruction for execution in an instruction cache in a processor in the data processing system, determining whether a performance indicator that identifies the execution of the instruction is to be monitored is present."

Appellant further states:

"[T]he Examiner asserts that matching the contents of the IABR to the executing instruction's address constitutes a 'performance indicator'. Specifically, in Heisch, the IABR is monitored to determine of a preselected address stored in the IABR equals an address of an instruction currently to be executed. An interrupt is caused if there is such a match. If the match itself is construed as comprising the performance indicator of claim 1, as proposed by the Examiner, such a match does not identify that execution of the instruction is to be monitored is present as recited in claim 1. In Heisch, all instructions are monitored and any 'indicator' that may be present in Heisch may indicate whether there is to be an interrupt, but does not indicate that execution of an instruction is to be monitored is present."

Appellant further states:

"Heisch does not disclose or suggest 'responsive to an access of data, determining whether a performance indicator that identifies that access of the data is to be monitored is present" Heisch never makes such a determination, and claim 8 is also not anticipated by Heish. Further, even if matching of the contents of the IABR to the address in question can be construed as comprising a performance indicator as suggested by Examiner, Heisch still does not disclose 'responsive to an access of data, determing whether a performance indicator that identifies that access of the data is to be monitored is present' as recited in claim 8."

Within the argument section, Appellant correctly describes the functionality of Heisch (aside from one important detail, described below). So, the distinction of these arguments appears to be how the invention of Heisch relates to the claims.

Appellant discloses several times within the arguments a citation of claims 1 and 8 that allegedly does not exist in Heisch. The argument appears to come down to one

determination: whether the performance indicator identifies that the execution of the instruction is to be monitored.

When making evaluations about a processing system, using every-day terminology like "identify" and relating it to a computer can often be rather difficult. The American Heritage Dictionary 4th Edition does not, as one might expect, have a "computer architecture" definition of the word "identify"; however, the first general definitions listed are "to recognize or establish as being a particular person or thing" and "verify the identity of".

The first definition appears to clearly be in support of the current rejection. The performance indicator of Heisch (of which Appellant does not admit or deny the existence—see page 12 of the Appeal Brief) is only required to recognize the existence of performance monitoring or, as it relates to a processor, show that the existence of performance monitoring has some effect on the performance indicator.

Here, this is clearly the case. As Applicant correctly describes in page 12 of the Appeal Brief, in Heisch "the IABR is monitored to determine if a preselected address stored in the IABR equals an address of an instruction currently to be executed. An interrupt is caused if there is such a match." Additionally, as described in the final Office Action on page 3, "The examiner asserts that matching the contents of the IABR register to the executing instruction's address constitutes a 'performance indicator'". Therefore, to satisfy the definition of "identify" it is simply required that the performance indicator recognize that such a match occurred and to act appropriately as a result (in the case of Heisch, by raising an interrupt as a result of such a match). By satisfying

this definition, the rejection under Heisch correctly satisfies the "broadest reasonable interpretation" requirement of 35 U.S.C. 102.

Appellant, based on the arguments presented, appears to desire that the definition of "identify" be narrowed. In particular, note the second definition given of identify: "verify the identity of". Appellant, it seems, believes that a definition, such as this one, implies a further requirement for identification—in particular, that the "thing" being identified cannot always exist. Examiner concedes that this second definition of "identify" does appear to carry that additional requirement.

Despite the fact that the first definition of "identified" supports the current rejection (therefore, making it reasonably interpreted), a further analysis will be provided. Appellant states that, "In Heisch, all instructions are monitored and any 'indicator' that may be present in Heisch may indicate whether there is to be an interrupt, but does not indicate that execution of an instruction is to be monitored is present." This statement is false. All instructions in Heisch are not monitored. Monitoring is not always enabled. This is clear from the summary of Heisch, "By coupling the performance monitor and IABR functionality, the performance monitor may thereby be enabled and disabled on a per instruction address basis" (Heisch col 4 lines 4-7).

Therefore, the limitation in question is satisfied by Heisch based on two distinct definitions of "identify"—the satisfaction of either one of them making the rejection proper.

Appellant's arguments with respect to the obvious rejections under 35 U.S.C. 103 appear to address the same arguments as shown above.

Appellant states:

"[Regarding the rejection under 35 U.S.C. 101, c]laims 21-25 recite clearly functional descriptive material since they impart functionality when employed as a computer component. Moreover, the functional descriptive material of claims 21-25 is recorded on 'some' computer-readable medium. In the above context, the term 'some' means 'any' computer-readable medium. The MPEP does not draw any distinctions between one type of media that is considered to be statutory and another type of media that is considered to be non-statutory. To the contrary, the MPEP clearly states that as long as the functional descriptive material is in 'some' computer-readable medium, it should be considered statutory."

Examiner disagrees. The claimed subject matter—"computer readable media"—when written in light of the specification includes transmission-type media. Transmission media are not tangible, and hence, non-statutory. The rejection is proper. Appellant is required to amend claims 19-25 to read "a computer program product in a computer readable recordable-type medium" in order to clarify the claims to be related to exclusively statutory subject matter.

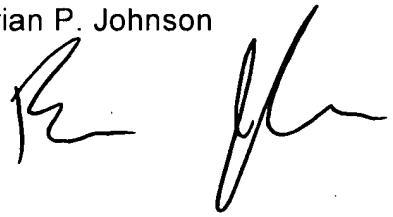
(11) Related Proceeding(s) Appendix

No decision rendered by a court or Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejection should be sustained.

Respectfully submitted,

Brian P. Johnson



07 December 2006

Conferences:

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